APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,380	06/30/2003	Roni Rosner	42P17037	1513

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EXAMINER
JOHNSON, BRIAN P

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/611,380	ROSNER ET AL.
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16, June 2006*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-21 are pending.

Papers Filed

2.   Examiner acknowledges receipt of remarks and amended claims, all filed June

16th, 2006.

Claim Objections

3.   Objections withdrawn.

Original Rejections

4.   Applicant has failed to overcome the prior art rejections set forth in the previous

Office Action. Consequently, these rejections are respectfully maintained by the

examiner and are copied below for applicant's convenience.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6.   Claims 6-21 are rejected under 35 U.S.C. 102(e) as being anticipated by

Strombergson et al. (U.S. Patent No. 6,807,621) hereinafter referred to as

Strombergson.

7.   As per claim 6, Strombergson discloses a method comprising:

        tracking the program order of a first set of instructions assigned to a first

local reorder buffer (Fig. 1 reservation unit 3A in combination with execution unit

4A) in a first execution unit (Fig. 1 reservation unit 3A in combination with

execution unit 4A);

        tracking the program order of a second set of instructions assigned to a

second local reorder buffer (Fig. 1 reservation unit 3B in combination with

execution unit 4B) in a second execution [unit] (Fig. 1 reservation unit 3B in

combination with execution unit 4B);

        and tracking program order of the first set of instructions relative to the

second set of instructions in a global reorder buffer (Fig. 1 commit stage 5). *The*

examiner asserts that since the commit stage contains a reorder buffer (ROB

10), the stage is responsible to for tracking program order from all the execution

stages.

8.   As per claim 7, Strombergson discloses the method of claim 6, further

comprising:

notifying the global reorder buffer (Fig. 1 commit stage 5) when a

mispredicted instruction occurs; (Col. 3 lines 34-60)

intiating a flush operation in the global reorder buffer (Fig. 1 commit stage

5); (Col. 3 lines 34-60)

and notifying the first local reorder buffer (Fig. 1 reservation unit 3A in

combination with execution unit 4A) of the mispredicted instruction. (Col. 3, lines

34-60)

9.   As per claim 8, Strombergson discloses the method of claim 7, further

comprising: notifying a fetch control unit (Fig. 1 fetch unit 1 in combination with decode

unit 2) of a mispredicted set of instructions. (Col. 3 line 51)

10.   As per claim 9, Strombergson discloses the method of claim 6, further

comprising: sending a signal to the second local reorder buffer (Fig. 1 reservation unit

3B in combination with execution unit 4B) to flush at least a third set of instructions.

(Col. 3 line 58-60)

11.   As per claim 10, Strombergson discloses the method of claim 6, further

comprising: fetching a fourth set of instructions; and assigning the fourth set of

instruction to the first reorder buffer during a flushing operation. *The examiner asserts*

that the processor will continue to process instructions, starting with the branch target

instruction, after a conditional branch has been taken. These instructions will be issued

to the functional stages, including the stage including the first reorder buffer, and will be executed once the flushing of the stage has been completed.

12.   As per claim 11, Strombergson discloses the method of claim 6, further comprising: retiring an instruction according to an indicator stored in the global reorder buffer(Fig. 1 commit stage 5). (Col. 8 lines 22-27) *The examiner asserts that indicators must exist to reorder instructions after execution.*

13.   As per claim 12, Strombergson discloses a system comprising:

       a bus; (Fig. 1, line connecting memory 7 to fetch unit 1)

       a memory device coupled to the bus; (Fig. 1 memory 7)

       and a processor including a fetch control unit (Fig. 1 fetch unit 1 and decode unit 2) to fetch instructions from the memory device, a first execution unit (Fig. 1 reservation unit 3A in combination with execution unit 4A) to process one or more of the fetched instructions, a second execution unit (Fig. 1 reservation unit 3B in combination with execution unit 4B) to process one of more of the fetched instructions, a first reorder buffer (Fig. 1 reservation unit 3A in combination with execution unit 4A) to track instructions assigned to the first execution unit, a second reorder buffer (Fig. 1 reservation unit 3B in combination with execution unit 4B) to track instructions assigned to the second execution unit, and a global reorder buffer (Fig. 1 commit stage 5) to track instruction order of instructions assigned to the first reorder buffer relative to the second reorder

buffer. (Col. 8 lines 22-27) *The examiner asserts that the reservation station in combination with the execution unit track a given instruction as it waits to be, and is finally executed. The examiner asserts that the reorder buffer 10 in commit stage 5 tracks the order of instructions as it retires instructions in their proper order.*

14.   As per claim 13, Strombergson discloses the system of claim 12, wherein the first reorder buffer is operable to signal the global reorder buffer upon detection of a mispredicted instruction. (Col. 3 lines 34-60)

15.   As per claim 14, Strombergson discloses the system of claim 12, wherein the first reorder buffer is operable to flush a first set of instructions upon detection of a mispredicted instruction (Col. 3 lines 34-60), and wherein the fetch control unit assigns a second set of instructions to the first reorder buffer based on a set of load balancing criteria. *The examiner asserts that the processor will continue to process instructions, starting with the branch target instruction, after a conditional branch has been taken. These instructions will be issued to the functional stages, including the stage including the first reorder buffer, and will be executed once the flushing of the stage has been completed.*

16.   As per claim 15, Strombergson discloses a machine readable medium having

stored therein instructions, which when executed cause a machine to perform a set of

operations comprising:

  tracking the program order of a first set of instructions assigned to a first

local tracking device in a first execution unit (Fig. 1 reservation unit 3A in

combination with execution unit 4A); *The examiner asserts that the reservation*

station in combination with the execution unit track a given instruction as it waits

to be, and is finally executed.

  tracking the program order of a second set of instructions assigned to a

second local tracking device in a second execution unit (Fig. 1 reservation unit

3B in combination with execution unit 4B); *The examiner asserts that the*

reservation station in combination with the execution unit track a given instruction

as it waits to be, and is finally executed.

  and tracking program order of the first set of instructions relative to the

second set of instructions in a global tracking device. (Fig. 1 commit stage 5) *The*

examiner asserts that the reorder buffer 10 in commit stage 5 tracks the order of

instructions as it retires instructions in their proper order.

17.   As per claim 16, Strombergson discloses the machine readable medium of claim

15, having further instructions stored therein which when executed cause a machine to

perform a set of operations further comprising: notifying the global tracking device (Fig.

1 commit stage 5) when a mispredicted instruction occurs. (Col. 3 line 55-57)

18.   As per claim 17, Strombergson discloses the machine readable medium of claim

16, having further instructions stored therein which when executed cause a machine to

perform a set of operations further comprising: tracking a first set of switch points in the

global tracking device (Fig. 1 commit stage 5). *The examiner further asserts that the*

reorder buffer 10 tracks a given instruction compared to prior and subsequent

instructions to maintain proper instruction ordering.

19.   As per claim 18, Strombergson discloses the machine readable medium of claim

16, having further instructions stored therein which when executed cause a machine to

perform a set of operations further comprising: flushing a second set of switch points

based on the mispredicted instruction. *The examiner asserts that when a conditional*

branch instruction is mispredicted, instructions currently in other stages of the pipeline

are flushed as described in col. 3 lines 34-60.

20.   As per claim 19, Strombergson discloses an apparatus comprising:

          a means for tracking the program order of a first set of instructions

assigned to a first local tracking device (Fig. 1 reservation unit 3A in combination

with execution unit 4A) in a first execution unit (Fig. 1 reservation unit 3A in

combination with execution unit 4A); *The examiner asserts that the reservation*

station in combination with the execution unit track a given instruction as it waits

to be, and is finally executed.

a means for tracking the program order of a second set of instructions

assigned to a second local tracking device (Fig. 1 reservation unit 3B in

combination with execution unit 4B) in a second execution unit (Fig. 1 reservation

unit 3B in combination with execution unit 4B); *The examiner asserts that the*

reservation station in combination with the execution unit track a given instruction

as it waits to be, and is finally executed.

and a means for tracking program order of the first set of instructions

relative to the second set of instructions in a global tracking device. (Fig. 1

commit stage 5) *The examiner asserts that the reorder buffer 10 in commit stage*

5 tracks the order of instructions as it retires instructions in their proper order.

21.   As per claim 20, Strombergson discloses the apparatus of claim 19, further

comprising: a means for notifying the global tracking device when a mispredicted

instruction occurs. (Col. 3 lines 34-60)

22.   As per claim 21, Strombergson discloses the apparatus of claim 19, further

comprising: a means for flushing at least a third set of instructions in the first local

tracking device. (Col. 3 lines 34-60)

Previously Presented Rejections

Claim Rejections - 35 USC § 101

23.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Rejection under 35 USC 101 has been withdrawn.

Claim Rejections - 35 USC § 102

24.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

25.   Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Strombergson.

26.   As per claim 1, Strombergson discloses a device comprising:

a first device (Fig. 1 reservation unit 3A in combination with execution unit 4A) to track segment order associated with a first execution unit (Fig. 1 execution unit 4A);

a second device (Fig. 1 reservation unit 3B in combination with execution unit 4B) to track segment order associated with a second execution unit (Fig. 1 execution unit 4B); *The examiner asserts that a single instruction constitutes a segment of the program running on Strombergson's processor. Further, the examiner asserts that the reservation unit 3A/B receives instructions intended for execution unit 4A/B. The*

reservation unit tracks instructions. Col. 4 lines 45-51 dictate that instructions are

checked for irregularities in the order that they were received at the decode stage. The

reservation unit must inherently track instruction order if it is to check for irregularities in

the proper order.

and a third device (Fig. 1 commit stage 5) coupled to the first device and second

device to track relative segment order between the first device and the second device.

The examiner asserts that the commit stage is coupled to the first and second execution

and reservation units as pictured in Fig. 1. Further, the reorder buffer must track

instructions through all execution units. If the reorder buffer did not keep track of

instruction order, instructions would not be guaranteed to complete in the proper order,

causing undesired operation of the processor.

27.   As per claim 2, Strombergson discloses the device of claim 1, wherein the first

device (Fig. 1 reservation unit 3A in combination with execution unit 4A) is operable to

notify the third device (Fig. 1 commit stage 5) of a mispredicted instruction in a segment,

and wherein the first device is operable to flush a first segment. (Col. 3 lines 34-60)

28.   As per claim 3, Strombergson discloses the device of claim 2, wherein the third

device (Fig. 1 commit stage 5) is operable to notify the second device (Fig. 1

reservation unit 3B in combination with execution unit 4B) of the mispredicted instruction

in the segment, and wherein the second device is operable to flush a second segment.

(Col. 3 lines 34-60)

29.   As per claim 4, Strombergson discloses the device of claim 2, wherein the third

device (Fig. 1 commit stage 5) is operable to notify the first device (Fig. 1 reservation

unit 3A in combination with execution unit 4A) of the mispredicted instruction in the

segment, and wherein the first device is operable to flush a third segment. (Col. 3 lines

34-60)

30.   As per claim 5, Strombergson discloses the device of claim 1, further comprising:

a fetch control unit (Fig. 1 fetch unit 1 in combination with decode unit 2) to predict

segment order (Col. 4 line 57-58), fetch segments and assign the segments to one of

the first device and the second device during a flush operation. (Col. 7 lines 42-54)

Response to Arguments

31.   Objections to claims are withdrawn in favor of amendments filed 16 June 2006.

32.   Rejection under 35 USC 101 has been withdrawn in favor of the amendments

filed 16 June 2006.

33.   Applicant's arguments filed on 16 June 2006 have been fully considered but they

are not persuasive.

Applicant states:

"Claim 6 includes the elements 'tracking program order of the first set of instructions relative to the second set of instructions in a global reorder buffer.' Applicants believe that Strombergson does not teach these elements of claim 6. The Examiner asserts that because 'the standard reorder buffer maintains a queue entry for each pending instruction on the processor,' that '[the buffer] keeps track of all instructions which have not yet been committed.' Nevertheless, this interpretation of Strombergson fails to teach 'tracking program order of the first set of instructions relative to the second set of instructions in a global reorder buffer.'"

Examiner disagrees. The following facts below are all that are required to reach

a conclusion that supports the maintained rejection:

1) The processing system reads a program that contains a list of instructions that

are initially in program order.

2) These instructions are separated into multiple local buffers (in particular 3A

and 3B of figure 1), wherein these buffers together obtain every instruction and do not

share instructions.

3) A global buffer (in particular, commit stage 5 of figure 1) must obtain each of

the instructions previously contained in the local buffers. The contents of these local

buffers must be merged precisely back into the program order for the processor to work

appropriately.

Conclusion: The relative order must be tracked; otherwise, these instructions

could not possibly be merged back into the original program order.

If there is any flaw in the logic above, Applicant is invited to address it in the next

response.

Applicant states:

"Consider figures 1-4, where there are no lines of communication between the commit stage 5 and instruction fetch stage 1, decoding stage 2 or any of the reservation units. Furthermore, execution 4a-4c have only one-way communications with commit stage 5 and only the instructions themselves are sent down these paths. Additionally, in col. 9, lines 5-16, Stromberson explains that the only way to set

the commit stage to flush mode is by marking the instruction itself...Without more communication, there is no way for the reorder buffer to track relative segment order between execution units. This further emphasizes that the only way for the rest of the system to communicate with the commit stage is to mark the instructions themselves before the commit stage receives them. Thus, in Strombergson the commit stage has no way to 'track' the instructions while they are in the reservation or execution units because the commit stage only knows where the instructions are once it receives the instructions after they have gone through the execution units. The commit stage cannot know which execution unit the instructions are in when they are in the execution units."

Examiner disagrees with several of the points made by Applicant.

1) Figures 1-4 in no way suggest that they are representative of all communications between any of the modules listed. Examiner asserts that for correct processor functionality, there are many lines of communication between the pluralities of stages.

2) Strombergson does discuss marking instructions that are to be flushed; however, Strombergson in no way states that this is the only way to complete this action. Additionally, this "marking" of instructions is considered to be a line of communication.

3) If it is true, as Applicant asserts, that the "commit stage has no way to track the instructions while they are in the reservation or execution units", then Examiner does not understand how the instructions are merged precisely in program order for them to be properly committed. Examiner asserts that instructions cannot be committed to an architectural state in any random order. Programmers write the instructions in a very precise order to ensure that logical dependencies are appropriately accounted for. If this order were disrupted in the commit stage, the program would not run correctly.
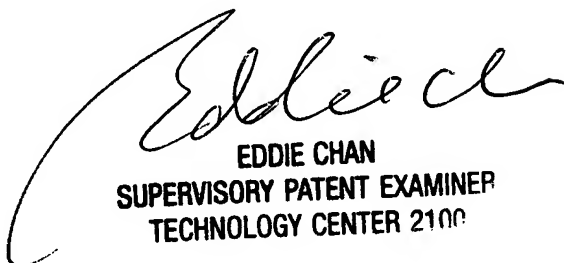
Conclusion

1.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-

2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

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USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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